NASA-DoD Lead-Free Electronics Project

Joint Test Protocol (JTP)

October 08, 2007

Preface

This report was prepared on behalf of, and under guidance provided by, the National Aeronautics and Space Administration (NASA) Technology Evaluation for Environmental Risk Mitigation (TEERM) Principal Center. The structure, format, and depth of the report's technical content were determined by the Working Group, government technical representatives, and government contractors in response to the specific needs of this project.

The data generated from the testing outlined in this document will be reported in the Joint Test Report (JTR) to be published following the completion of all testing activities.

Invaluable technical, business, and programmatic contributions were provided by the organizations listed below.

- BAE Systems
- Boeing
- CALCE
- Celestica
- COM DEV
- DMEA
- F-15 Program Office
- Harris
- Honeywell
- Lockheed Martin
- NASA Jet Propulsion Lab
- NASA Marshall Space Flight Center
- NAVSEA Crane
- Nihon Superior
- Raytheon
- Rockwell Collins
- Texas Instruments
- TT Apsco
- Warner Robins Air Logistics Center, Robins Air Force Base

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1.0 Applicable Documents

- IPC 6012B: Qualification and Performance Specification of Printed Circuit Boards Amendment 1 January 2007
- IPC 45101B: Specification for Base Materials for Rigid and Multilayer Printed Boards, Amendment 1 February 2007
- MIL-STD-810F: Environmental Engineering Considerations and Laboratory Tests January 2000
- IPCA J-STD-001D: Requirements for Soldered Electrical and Electronic Assemblies February 2005
- IPC SM-785: Guidance for Accelerated Reliability Testing of Surface Mount Solder Attachments Nov. 1992
- IPC-9701A: Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments February 2006
- IPC TM 650:
- NASA STD 8739.2: Workmanship Standard for Surface Mount Technology
- IPC 9252: Guidelines and Requirements for Electrical Testing of Unpopulated Boards, February 2001
- ANSI/J-STD-003B: Solderability Test for Printed Boards, March 2007
- IPC-2221A: Generic Standard on Printed Board Design, May 2003
- IPC-2222: Sectional Design Standard for Rigid Organic Printed Boards, February 1998
- IPC-A-610D: Acceptability of Electronic Assemblies, February 2005
- IPC-4101B: Specification for Base Materials for Rigid and Multilayer Printed Boards, June 2006

2.0 Introduction

2.1 Lead-Free Solder Overview

The use of conventional tin-lead (SnPb) in circuit board manufacturing is under ever-increasing political scrutiny due to increasing regulations concerning lead. The "Restriction of Hazardous Substances" (RoHS) directive enacted by the European Union (EU) and a pact between the United States National Electronics Manufacturing Initiative (NEMI), Europe's Soldertec at Tin Technology Ltd. and the Japan Electronics and Information Technology Industries Association (JEITA) are just two examples where worldwide legislative actions and partnerships/agreements are affecting the electronics industry. As a result, many global commercial grade electronic component suppliers are initiating efforts to transition to lead-free (LF) in order to retain their worldwide market. Lead-free components are likely to find their way into the inventory of aerospace or military assembly processes under current government acquisition reform initiatives. Inventories contaminated by lead-free will result in increased risks associated with the manufacturing, product reliability, and subsequent repair of aerospace and military electronic systems.

Although electronics for military and aerospace applications are not included in the RoHS legislation, engineers are beginning to find that the commercial industry's move towards RoHS compliance has affected their supply chain and changed their parts. Most parts suppliers plan to phase out their non-compliant, leaded production and many have already done so. As a result, the ability to find leaded components is getting harder and harder. Some buyers are now attempting to acquire the remaining SnPb inventory, if it's not already obsolete.

The introduction of components with lead-free terminations, termination finishes, or circuit boards presents a host of concerns to customers, suppliers, and maintainers of aerospace and military electronic systems such as:

- Electrical shorting due to tin whiskers
- Incompatibility of lead-free processes and parameters (including higher melting points of lead-free alloys) with other materials in the system
- Unknown material properties and incompatibilities that could reduce solder joint reliability

Original Equipment Manufacturers (OEMs), depots, and support contractors have to be prepared to deal with an electronics supply chain that increasingly provides more and more parts with lead-free finishes—some labeled no differently than their Pb counterparts—while at the same time providing the traditional Pb parts. The longer the transition period, the greater the likelihood of lead-free parts inadvertently being mixed with Pb parts and ending up on what are supposed to be Pb systems. As a result, OEMs, depots, and support contractors need to take action now to either abate the influx of lead-free parts, or accept it and deal with the likely interim consequences of reduced reliability due to wide variety of matters, such as Pb contamination, high temperature incompatibility, and tin whiskering.

2.2 Project Approach

Allowance of lead-free components produces one of the greatest risks to the reliability of a weapon system. This is due to new and poorly understood failure mechanisms, as well as unknown long-term reliability. If the decision is made to consciously allow lead-free solder and component finishes into SnPb electronics, additional effort (and cost) will be required to make the significant number of changes to drawings and task order procedures.

Lead-free alloys have higher melting temperatures than tin-lead, which can cause problems for those who use lead-free parts in manufacturing. Some part suppliers provide data about reflow temperatures, but others provide little or no information. This affects both OEMs and repair facilities, as a backward-compatibility problem may be discovered only when the product fails.

OEMs and military depots have indicated that they have received lead-free components even after steps had been taken to avoid this scenario. The extent to which lead-free has been introduced into SnPb systems for high reliability applications is unknown, but as more suppliers transition to lead-free the risk of contamination is expected to increase.

As the transition to lead-free becomes an ever closing reality for military and aerospace applications, it will be critical to fully understand the implications of reworking lead-free assemblies. The intended goal of this project is to:

- Determine the reliability of reworked solder joints in high-reliably military and aerospace electronics assemblies.
- Assess the process parameters for reworking high-reliability lead-free military and aerospace electronics assemblies.
- Develop baseline recommendations for process guideline and risk assessment for assembling high-reliability lead-free military and aerospace electronics assemblies

3.0 Engineering and Testing Requirements

This section summarizes the engineering and testing requirements for the "Manufactured" and "Rework" test vehicles.

"Manufactured"(Mfg.) test vehicles represent printed wiring assemblies newly manufactured for use in new product. Test vehicles being subjected to thermal cycle and combined environments testing will include forward and backward compatibility. Test vehicles assembled for vibration and mechanical shock will not include forward and backward compatibility. The "Manufactured" test vehicles were assembled using immersion silver (Ag) and a limited number of electroless nickel / immersion gold (ENIG) finished glass fiber (GF) laminate (IPC-4101/26) printed circuit boards with a glass transition temperature, T_g, of 170°C minimum.

The "Rework" (Rwk.) test vehicles represent printed wiring assemblies manufactured and reworked prior to being tested. Solder mixing (SnPb/lead-free & lead-free/SnPb) will be evaluated on all "Rework" test vehicles. The "Rework" test vehicles were assembled using immersion silver (Ag) and a limited number of electroless nickel / immersion gold (ENIG) finished glass fiber (GF) laminate (IPC-4101/26) printed circuit boards with a glass transition temperature, T_g, of 170°C minimum.

For this document, forward and backward compatibility have been defined as:
- Forward Compatibility is a SnPb component attached to a printed wiring assembly using lead-free solder with a lead-free profile.
- Backward compatibility is a lead-free component attached to a printed wiring assembly using SnPb solder with a SnPb solder profile.

Tests contained in this JTP may involve the use of hazardous materials. However, this JTP does not address safety issues associated with their use. Therefore, when performing tests described in this JTP, appropriate safety and health practices must be established, and the applicability of regulatory limitations must be determined.

3.2 Test Vehicle- Printed Wiring Assembly

The test vehicle for most tests in this JTP (except where noted) is a printed wiring assembly (PWA), designed to evaluate solder joint reliability. Test vehicle raw boards shall comply with IPC-6012 (Qualification and Performance Specification for Rigid Printed Boards), Class 3, Type 3. Test vehicle size will be 14.5 X 9 X 0.09 inches with six 0.5-ounce copper layers. The design incorporates components representative of the parts used for military and aerospace systems and is designed to reveal relative differences in solder alloy performance.

The test vehicle will include a variety of plated through-hole (PTH) and surface mount technology (SMT) components. All components will be "dummy" devices with pins internally daisy-chained and will contain simulated die. The circuit board will be designed with daisy-chained pads that are complementary to the components, except for the chip capacitors. Therefore, the solder joints on each component will be part of a continuous electrical pathway that can be monitored during testing by an event detector (Anatech or equivalent). Failure of a solder joint on a component will break the continuous pathway and be recorded as an event. Each component will have its own distinct pathway (channel).

3.3 Quality conformance of Printed Circuit Boards (PCB) for the Test vehicle

The PCBs for testing shall be supplied from one production lot, and inspected per the requirements of IPC 6012 Class 3. Test coupons shall be evaluated by cross sectioning and /or per PWB Interconnect Solutions Inc Testing philosophy per IPC 9252 Guidelines.

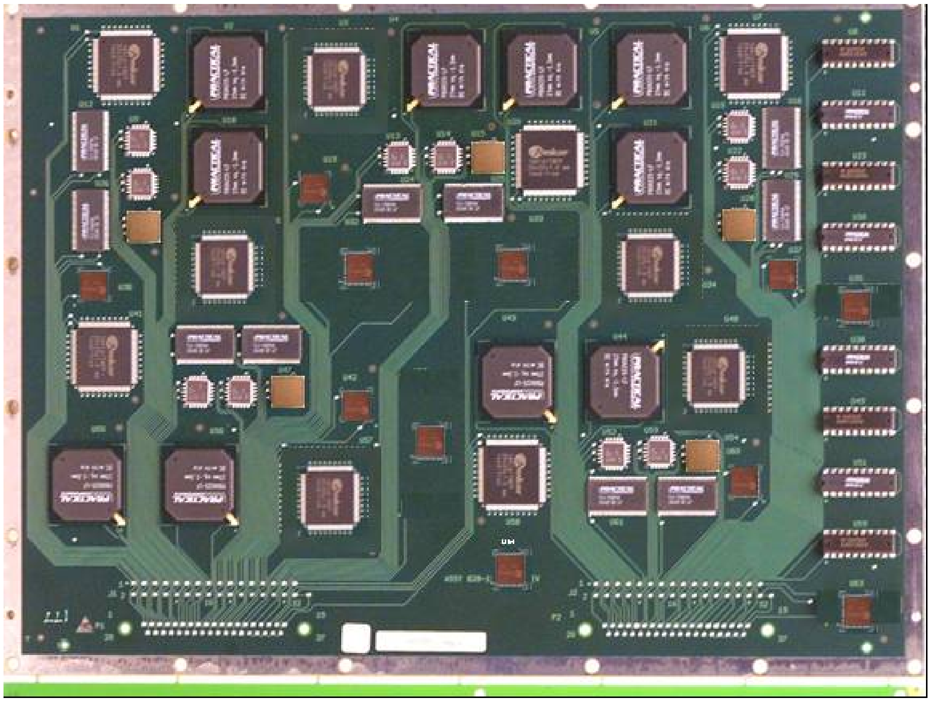


Figure 1 NASA-DoD LFE Project Test Vehicle
Note: Figure 1 will be updated once the test vehicle assembly is complete

3.4 General Inspection Procedures

3.4.1 Pre-Test Inspection

Visual inspection and photographs will document the visual appearance of the solder joints prior to testing. Deviations from IPC J-STD-001 Revision D, Class 3 (*Requirements for Soldered Electrical and Electronic Assemblies*) will be noted. X-ray will be used to document solder ball alignment and voiding. Prior to assembly, board finishes and component finishes must be verified by energy dispersive X-ray (EDX) or X-ray fluorescence (XRF). Prior to assembly, a few components of each type should be tested, using an ohmmeter, to ensure they are daisy-chained internally.

3.4.2 **Post-Test Inspection**

Visual inspection and photographs will document the visual appearance of the solder joints after testing is completed. Assembled test vehicles will be set aside for cross sections, and will not undergo testing. Cross sections will be done to document post-test metallography and measure solder joint height, and ball grid array (BGA) and chip scale package (CSP) solder ball alignment.

3.5 Engineering, Performance

The performance requirements and related tests for PWAs are listed in Table 1. These tests are required by all military and aerospace systems that participated in the development of this JTP. Both "Manufactured" and "Rework" PWAs will be subjected to all common tests.

Table 1 Performance Requirements

Test Procedure	JTP Section	Reference	Electrical Test	Acceptance Criteria [(a)]
Vibration	4.2.1	MIL-STD-810F, Method 514.5, Procedure I	Electrical continuity failure	Better than or equal to SnPb controls
Mechanical Shock	4.2.2	MIL-STD-810F, Method 516.5	Electrical continuity failure	Better than or equal to SnPb controls
Thermal Cycling	4.2.3	IPC-SM-785	Electrical continuity failure	Better than or equal to SnPb controls at 10%[b] Weibull cumulative failures
Combined Environments Test	4.2.4	MIL-STD-810F Method 520.2 Procedure I	Electrical continuity failure	Better than or equal to SnPb controls at 10%[b] Weibull cumulative failures
Drop Testing	4.2.5	JEDEC Standard JESD22-B110A	Electrical continuity failure	Better than or equal to SnPb controls
Interconnect Stress Test (IST)	4.2.6	IPC-TM-650-2.6.26	Electrical continuity testing	3 thermal cycles simulate assembly and 6 thermal cycles simulate assembly and rework
Copper Dissolution	4.2.7	IPC-TM-650-2.1.1 ASTM-E-3	Cross section/ metallographic analysis	N/A

[a] Failure of a test board in a specific test does not necessarily disqualify a lead-free solder alloy for use in an application for which that test does not apply. Electrical performance requirements for a particular circuit apply only to parts containing that circuit.

[b] 10% noncompliance of minimal Weibull distribution data for Thermal Cycling and Combined Environments Testing was selected because it was a compromise between the 63.2% failures which is taken as normal life, and 1% failures (or first failure) which is most important in high reliability systems.

3.6 Quality Assurance

Statistical considerations are essential for meaningful conclusions that will hold up under scrutiny. The quantity of components on the test vehicle and the test sample sizes have been selected to provide statistically meaningful results.

Statistical review of the data generated by the testing is of utmost importance to the project consortium. Statistical distribution of failures will be represented by a Weibull distribution. As the lead-free solder testing is performed and the solder joints fail, Weibull distribution coefficients will be determined for the data collected as discussed in IPC-9701, section 5.2. The data of most interest is the first solder joint failure; the number of cycles required to reach 63.2% failures (called the characteristic life or alpha); the failure free period; and the Weibull shape parameter (beta).

When one solder joint fails on a component, the whole component is considered failed. In order to generate useful Weibull plots, ideally 50% of the assemblies must fail with a 63.2% component failure rate preferred, which requires many testing cycles (many hundreds too many thousands depending on the type of component).

Project technical representatives discussed sample size at length. For those tests where five test vehicles are used, the sample size for each component type ranges from 20 - 30. To achieve a 90% confidence level at 10% cumulative failures, a minimum sample size of 21 is required. The stakeholder's felt that the selected sample sizes, rather than 32 as specified in IPC-9701, would provide statistically meaningful results. IPC-SM-785, Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments, has equations for calculating the minimum number of failure-free test cycles for a given cumulative failure probability percentage with sample size and design life cycle requirement.

4.0 Testing descriptions

This Section briefly describes those tests that will permit project participants to consider qualifying lead-free solder alloys. Where appropriate, the test descriptions include the number and type of test specimens per solder alloy, number of trials per specimen, any major or unique equipment, and data recording and calculation requirements.

4.1 Auxiliary Testing

4.1.1 Electrical Continuity Testing

The test vehicles will be wired directly to the event detector; connectors are not allowed on the test vehicles. An event detector (Anatech or equivalent conforming to IPC-SM-785) will be used to monitor the electrical continuity of each channel on the test vehicle, and thereby detect solder joint failures that occur during testing (i.e. an "event"). The failure criteria measured by the event detector will be 10 events per channel with an interruption of electrical continuity (≥300 Ω) for periods greater than 0.2 µsec per IPC-SM-785 (Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments).

Table 2 Electrical Continuity Testing

Failure Criteria	- 10 events per channel - 0.2 microsecond - ≥ 300 Ω resistance for thermal cycle - ≥ 300 Ω for mechanical shock and vibration

Major or Unique Equipment
- Event detector (Anatech or equivalent)

Data Recording and Statistical Analysis
- Record of failures

4.1.2 Coefficient of Thermal Expansion (CTE) Testing

Measure CTE of SMT components only and the test vehicle per IPC-TM-650, Method 2.4.41 (Coefficient of Linear Thermal Expansion for Electrical Insulating Materials). This method determines the coefficient of linear thermal expansion by use of thermo-mechanical analyzer (TMA). For area array devices, shadow moiré may be used for additional analysis. The measured CTE values will be representative of each component as a composite of its construction/configuration.

4.1.3 Component Height Testing

The component height off the printed wiring board of each SMT component type will be measured (IPC-TM-650-2.1.1) during the microsection examination of the finished vehicle assemblies set aside for post-test inspection.

4.2 Environmental Exposure and Physical Reliability Tests

4.2.1 **Vibration**

Description

This test quantifies solder joint failures on PWAs during exposure to vibration. The limits identified in vibration testing will be used to compare performance differences in the lead-free test alloys and mixed solder joints vs. the baseline standard SnPb (63/37) alloy.

This test will satisfy the general requirements of MIL-STD-810F (Test Method Standard for Environmental Engineering Considerations and Laboratory Tests) Method 514.5 (Vibration) and will be performed using the following procedure:

- Confirm the electrical continuity of each test channel prior to testing. One channel will be used per component.
- Place the PWAs into a test fixture in random order and mount the test fixture onto an electrodynamic shaker.
- Conduct a step stress test in the Z-axis only (i.e., perpendicular to the plane of the circuit board). Most failures will occur with displacements applied in the Z-axis as that will result in maximum board bending for each of the major modes.
- Run the test using the stress steps shown in Figure 2 and Table 3. Subject the test vehicles to 8.0 g_{rms} for one hour. Then increase the Z-axis vibration level in 2.0 g_{rms} increments, shaking for one hour per step until the 20.0 g_{rms} level is completed. Then subject the test vehicles to a final one hour of vibration at 28.0 g_{rms}.
- Continuously monitor the electrical continuity of the solder joints during the test using event detectors with shielded cables. All wires used for monitoring will be soldered directly to the test vehicles and then glued to the test vehicles (with stress relief) to minimize wire fatigue during the test.
- If feasible, a complete modal analysis should be conducted on one test vehicle using a laser vibrometer system in order to determine the resonant frequencies and the actual deflection shapes for each mode

The stakeholders agreed that a stress step test representing increasingly severe vibration environments was appropriate for this test. A step stress test is required since a test conducted at a constant 8.0 g_{rms} level (Step 1) would take thousands of hours to fail the same number of components as a step stress test. This is because some locations on a circuit assembly experience very low stresses and severe vibration is required in order to fail components at these locations. The shape of the PSD (Power Spectral Density) curve for each step stress level was designed so that all of the major resonances of the test vehicles would be excited by the random vibration input. The PSD curves presented in MIL-STD-810F were used as guides for the creation of this step stress test but were not directly duplicated.

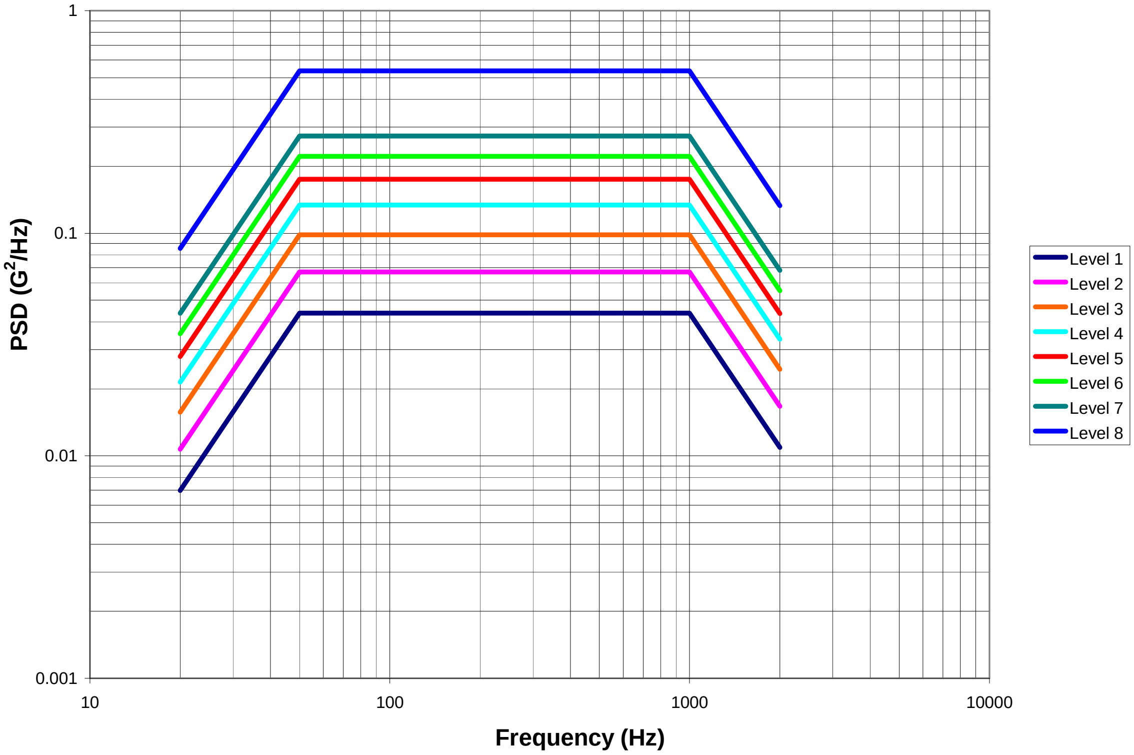


Figure 2 Vibration Spectrum

Table 3 Vibration Profile

Level 1	**Level 2**	**Level 3**
20 Hz @ 0.00698 G^2/Hz	20 Hz @ 0.0107 G^2/Hz	20 Hz @ 0.0157 G^2/Hz
20 - 50 Hz @ +6.0 dB/octave	20 - 50 Hz @ +6.0 dB/octave	20 - 50 Hz @ +6.0 dB/octave
50 - 1000 Hz @ 0.0438 G^2/Hz	50 - 1000 Hz @ 0.067 G^2/Hz	50 - 1000 Hz @ 0.0984 G^2/Hz
1000 - 2000 Hz @ -6.0 dB/octave	1000 - 2000 Hz @ -6.0 dB/octave	1000 - 2000 Hz @ -6.0 dB/octave
2000 Hz @ 0.0109 G^2/Hz	2000 Hz @ 0.0167 G^2/Hz	2000 Hz @ 0.0245 G^2/Hz
Composite = 8.0 G$_{rms}$	**Composite = 9.9 G$_{rms}$**	**Composite = 12.0 G$_{rms}$**

Level 4	**Level 5**	**Level 6**
20 Hz @ 0.0214 G^2/Hz	20 Hz @ 0.0279 G^2/Hz	20 Hz @ 0.0354 G^2/Hz
20 - 50 Hz @ +6.0 dB/octave	20 - 50 Hz @ +6.0 dB/octave	20 - 50 Hz @ +6.0 dB/octave
50 - 1000 Hz @ 0.134 G^2/Hz	50 - 1000 Hz @ 0.175 G^2/Hz	50 - 1000 Hz @ 0.2215 G^2/Hz
1000 - 2000 Hz @ -6.0 dB/octave	1000 - 2000 Hz @ -6.0 dB/octave	1000 - 2000 Hz @ -6.0 dB/octave
2000 Hz @ 0.0334 G^2/Hz	2000 Hz @ 0.0436 G^2/Hz	2000 Hz @ 0.0552 G^2/Hz
Composite = 14.0 G$_{rms}$	**Composite = 16.0 G$_{rms}$**	**Composite = 18.0 G$_{rms}$**

Level 7	**Level 8**
20 Hz @ 0.0437 G^2/Hz	20 Hz @ 0.0855 G^2/Hz
20 - 50 Hz @ +6.0 dB/octave	20 - 50 Hz @ +6.0 dB/octave
50 - 1000 Hz @ 0.2734 G^2/Hz	50 - 1000 Hz @ 0.5360 G^2/Hz
1000 - 2000 Hz @ -6.0 dB/octave	1000 - 2000 Hz @ -6.0 dB/octave
2000 Hz @ 0.0682 G^2/Hz	2000 Hz @ 0.1330 G^2/Hz
Composite = 20.0 G$_{rms}$	**Composite = 28.0 G$_{rms}$**

Rationale

The stakeholders felt that the general requirements of MIL-STD-810F, Method 514.5, (Vibration) are appropriate for determining how lead-free solder alloys perform under severe vibration. The vibration test will be run using the stress steps shown in Figure 2 and Table 3 developed specifically for the NASA-DoD Lead-Free Electronics Project by the Electronic, Electrical, and Electromechanical (EEE) Parts and Packaging Group of NASA Marshall Space Flight Center and Boeing. Project stakeholders agreed that a step stress vibration test was required in order to maximize the number of components that would fail during the test. A test conducted at a constant 8.0 g$_{rms}$ level would take thousands of hours to fail the same number of components as the step stress test.

Table 4 Vibration Test Methodology

<table>
<tr><td>Parameters</td><td colspan="6">- Start at 8.0 g_{rms} then step up in 2 g_{rms} increments in the axis perpendicular to the plane of the test vehicles until the 20.0 g_{rms} level is completed. Vibrate for 1 hour at each test level. Finish with 1 hour at 28.0 g_{rms}.</td></tr>
<tr><td colspan="7">Number of Test Vehicles Required</td></tr>
<tr><td colspan="4">Manufactured</td><td colspan="3">Rework</td></tr>
<tr><td>Mfg. SnPb</td><td>Mfg. LF</td><td>Mfg. LF ENIG</td><td>Mfg. LF SN100C</td><td>Rwk. SnPb</td><td>Rwk. SnPb ENIG</td><td>Rwk. LF</td></tr>
<tr><td>5</td><td>5</td><td>1</td><td>5</td><td>5</td><td>1</td><td>5</td></tr>
<tr><td colspan="3">Trials per Specimen</td><td colspan="4">1</td></tr>
</table>

<u>Major or Unique Equipment</u>

- Electrodynamic shaker
- Event detector (Anatech or equivalent)
- Fixture

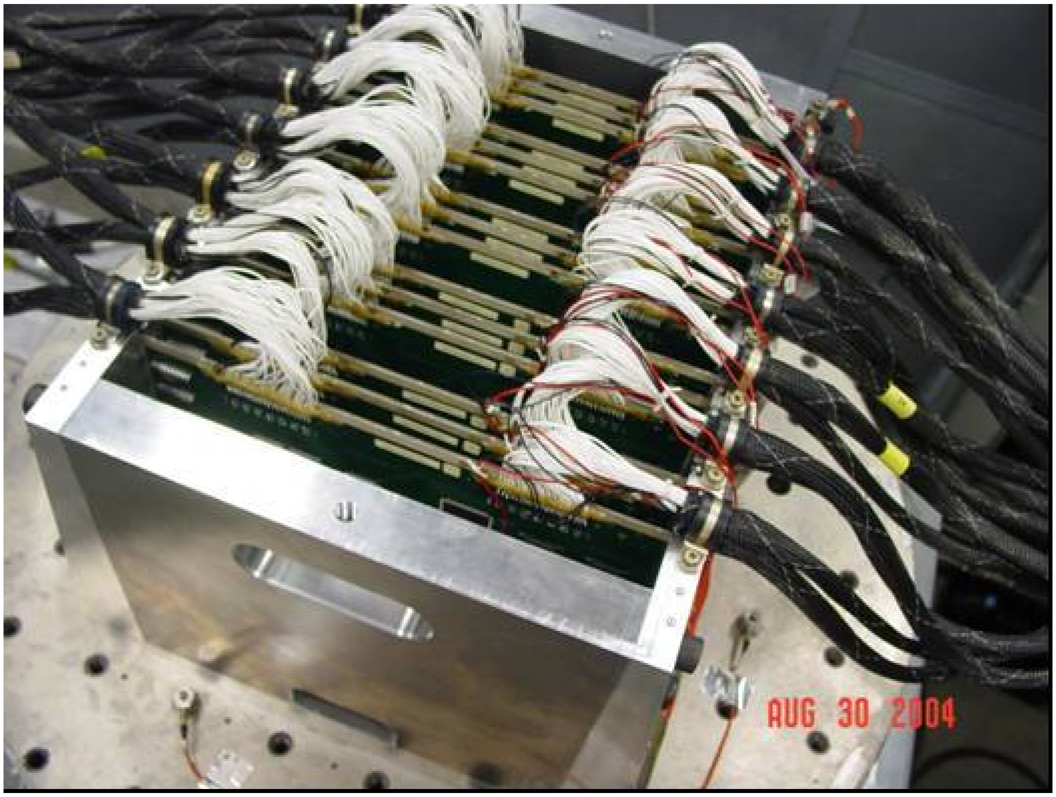


Figure 3 Vibration Test Fixture

<u>Data Recording and Calculations</u>

- Record data and compare to acceptance criteria as specified in JTP Section 4.1.1.

4.2.2 **Mechanical Shock**

Description

The purpose of this test is to determine the resistance of solders to the stresses associated with high-intensity shocks. Testing will be performed in accordance with the requirements specified in MIL-STD-810F (with modifications). A step stress shock test will be performed to maximize the number of failures generated which will allow comparisons of solder reliability to be made.

The PWAs will be mounted in a fixture on an electro-dynamic shaker. The required shock response spectrum (SRS) will be programmed into the digital shock controller which in turn will generate the required transient shock time history.

Testing will follow MIL-STD-810F, Method 516.5 with the following modifications: (1)100 shocks will be applied per test level (rather than 3) and all of the shocks will be applied in the Z-axis, and (2) the shock transients applied at the levels specified in MIL-STD-810F, Method 516.5 for the Functional Test for Flight Equipment, the Functional Test for Ground Equipment, and the Crash Hazard Test for Ground Equipment will follow the modified parameters given in Table 5. An additional step stress test will then be conducted (per Table 5 and Figure 4) with the shocks being applied in the Z-axis only. Testing will continue until a majority (approximately 63 percent) of components has failed. Shock levels, pulse durations and/or frequencies may be modified during testing based on the actual capabilities of the electrodynamic shaker used.

The test SRS shall be within +3dB and -1.5dB of the nominal requirement over a minimum of 90% of the frequency band when using a 1/12-octave analysis bandwidth. The remaining 10% of the frequency band shall be within +6dB and -3dB of the nominal requirement.

The electrical continuity of the solder joints will be continuously monitored during the test. All test results will be recorded

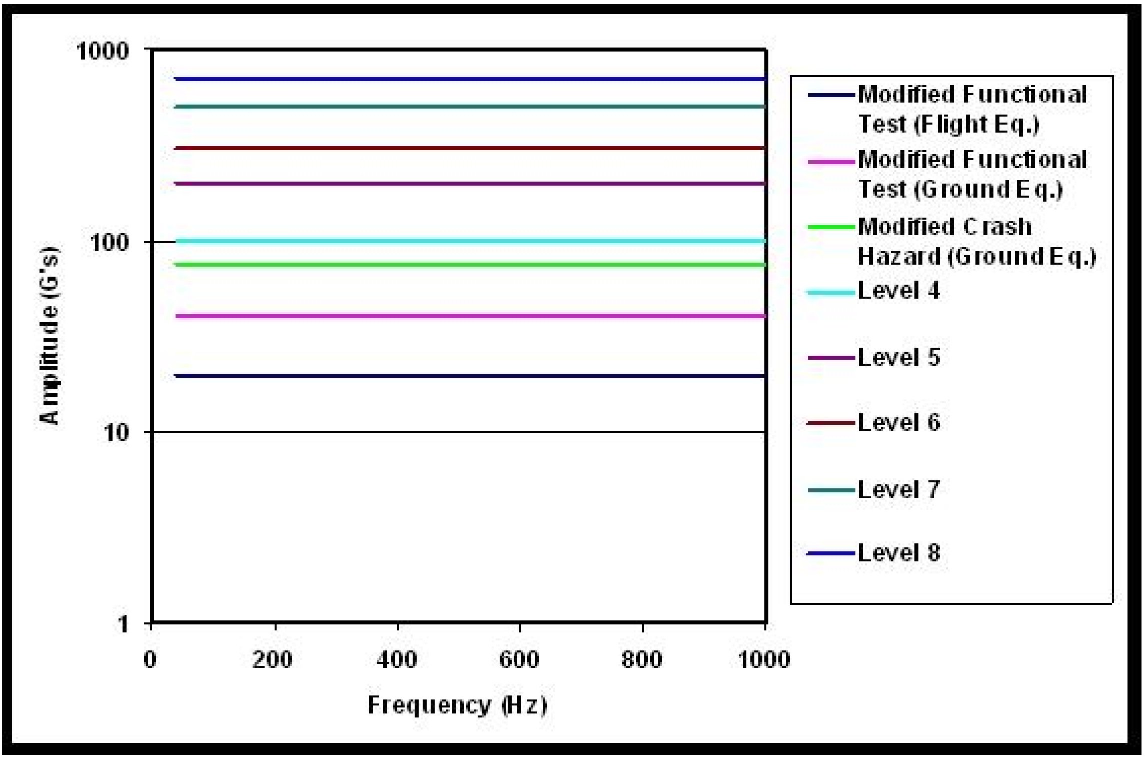


Figure 4 Mechanical Shock Response Spectrum

Rationale
The project stakeholders felt that MIL-STD-810F, Method 516.5, Procedure I (Functional Shock) is appropriate for determining how lead-free solder alloys perform under severe mechanical shock.

The stakeholders agreed that a stress step test representing different shock scenarios was necessary. The first three levels address the requirements of MIL-STD-810F. MIL-STD-810F, Method 516.5, Procedure I (Functional Shock) is intended to test material (including mechanical, electrical, hydraulic, and electronic) in its functional mode and to assess the physical integrity, continuity, and functionality of the material to shock. In general, the material is required to function during the shock and to survive without damage to shocks representative of those that may be encountered during operational service. The project representatives agreed that all three MIL-STD-810F shock levels (Functional Test for Flight Equipment, Functional Test for Ground Equipment, and Crash Hazard Test for Ground Equipment) should be used (with modification per Table 5) as they are representative of different field environments. The project representatives felt that only testing in the Z-axis was required as this is the only axis which allows significant board bending and subsequent solder joint failures. The representatives also felt that the number of shocks per test should be increased from 3 to 100 in order to increase the probability of failure at any one test level.

Additional step stress shock testing will then be performed to obtain as many failures as possible (Levels 4 through 8). One hundred shocks will be applied per level and the shocks will again be applied in the Z-axis only. These additional step stress levels were derived by NASA Jet Propulsion Laboratory and Boeing representatives.

Table 5 Mechanical Shock Test Methodology – Test Procedure

<table>
<tr><td rowspan="10">Parameters</td><td colspan="4">The shock transients will be applied perpendicular to the plane of the board and will be increased after every 100 shocks (i.e., a step stress test). Frequency range is 40 to 1000 Hz. SRS damping: 5%</td></tr>
<tr><td>Test Shock Response Spectra</td><td>Amplitude (G’s)</td><td>Te (msec)</td><td>Shocks per Level</td></tr>
<tr><td>Modified Functional Test for Flight Equipment (Level 1)</td><td>20</td><td><30</td><td>100</td></tr>
<tr><td>Modified Functional Test for Ground Equipment (Level 2)</td><td>40</td><td><30</td><td>100</td></tr>
<tr><td>Modified Crash Hazard Test for Ground Equipment (Level 3)</td><td>75</td><td><30</td><td>100</td></tr>
<tr><td>Level 4</td><td>100</td><td><30</td><td>100</td></tr>
<tr><td>Level 5</td><td>200</td><td><30</td><td>100</td></tr>
<tr><td>Level 6</td><td>300</td><td><30</td><td>100</td></tr>
<tr><td>Level 7</td><td>500</td><td><30</td><td>100</td></tr>
<tr><td>Level 8</td><td>700</td><td><30</td><td>100</td></tr>
<tr><td colspan="5">Number of Test Vehicles Required</td></tr>
<tr><td colspan="2">Manufactured</td><td colspan="3">Rework</td></tr>
<tr><td>Mfg. SnPb</td><td>Mfg. LF</td><td>Rwk. SnPb</td><td>Rwk. SnPb ENIG</td><td>Rwk. LF</td></tr>
<tr><td>5</td><td>5</td><td>5</td><td>1</td><td>5</td></tr>
<tr><td colspan="2">Trials per Specimen</td><td colspan="3">1</td></tr>
</table>

<u>Major or Unique Equipment</u>

- Shock table
- Event detector (Anatech or equivalent)
- Fixture

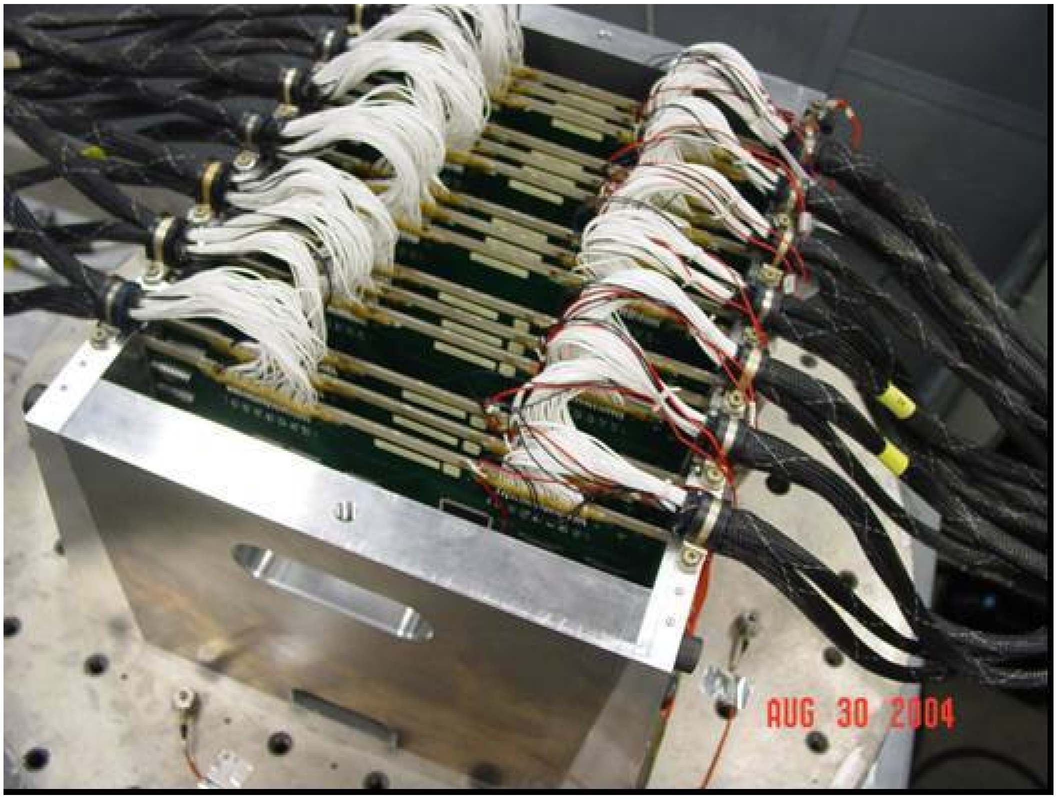


Figure 5 Mechanical Shock Test Fixture

Note, connectors are not to be used (hard wiring and adhesive staking is the accepted practice).

Data Recording and Calculations

- Record data and compare to acceptance criteria as specified in JTP Section 4.1.1.

4.2.3 Thermal Cycling

Description

This test determines a test specimen's resistance to degradation from thermal cycling. The limits identified in thermal cycle testing will be used to compare performance differences in the lead-free test alloys and mixed solder joints vs. the baseline standard SnPb (63/37) alloy.

Perform this test in accordance with IPC-SM-785 *(Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments)* and the following procedure.

- Continuously monitor the electrical continuity of the solder joints during the test. It is desirable to continue thermal cycling until 63% of each component type fails.

Table 6 Thermal Cycling Test Methodology; -20 to +80°C

Parameters	- -20 to +80°C - Cycles: The project consortia will review the data and determine when the test is complete - Decision point 10,000 cycles - 5 to 10°C/minute ramp - 30 minute high temperature dwell - 10 minute low temperature dwell			
Number of Test Vehicles Required				
Manufactured		Rework		
Mfg. SnPb	Mfg. LF	Rwk. SnPb	Rwk. SnPb ENIG	Rwk. LF
5	5	5	1	5
Trials per Specimen	1			

Table 7 Thermal Cycling Test Methodology; -55 to +125°C

<table>
<tr><td colspan="2">Parameters</td><td colspan="5">- -55 to +125°C
- Cycles: The project consortia will review the data and determine when the test is complete
- Decision point at 2,000 and 4,000 cycles
- 5 to 10°C/minute ramp
- 30 minute high temperature dwell
- 10 minute low temperature dwell</td></tr>
<tr><td colspan="7">Number of Test Vehicles Required</td></tr>
<tr><td colspan="4">Manufactured</td><td colspan="3">Rework</td></tr>
<tr><td>Mfg. SnPb</td><td>Mfg. LF</td><td>Mfg. LF SN100C</td><td>Mfg. LF ENIG</td><td>Rwk. SnPb</td><td>Rwk. SnPb ENIG</td><td>Rwk. LF</td></tr>
<tr><td>5</td><td>5</td><td>5</td><td>1</td><td>5</td><td>1</td><td>5</td></tr>
<tr><td colspan="2">Trials per Specimen</td><td colspan="5">1</td></tr>
</table>

Rationale

Two thermal ranges are required to produce data for model validation. Validated models will allow lifetime predictions to be made for electronics in actual use conditions. US Army Aviation and Missile Command (AMCOM) proposed temperature-cycling ranges of -55 to +125°C and -20 to +80°C. Although 1,000 temperature cycles may be enough for some Programs to certify a product, this will not result in enough component failures for model validation.

After examining the available data on dwell time effect, the lead-free solder project participants agreed that the high-temperature dwell time for the -55 to +125°C thermal cycles will be 30 minutes. Solder alloy creep during the high temperature dwell of the thermal cycle is largely responsible for damage within the solder joints. In order to maximize the effects of solder alloy creep, a 30-minute high temperature dwell will be used for this project.

Major or Unique Equipment

- Event detectors (Anatech or equivalent)
- Thermal cycle chambers

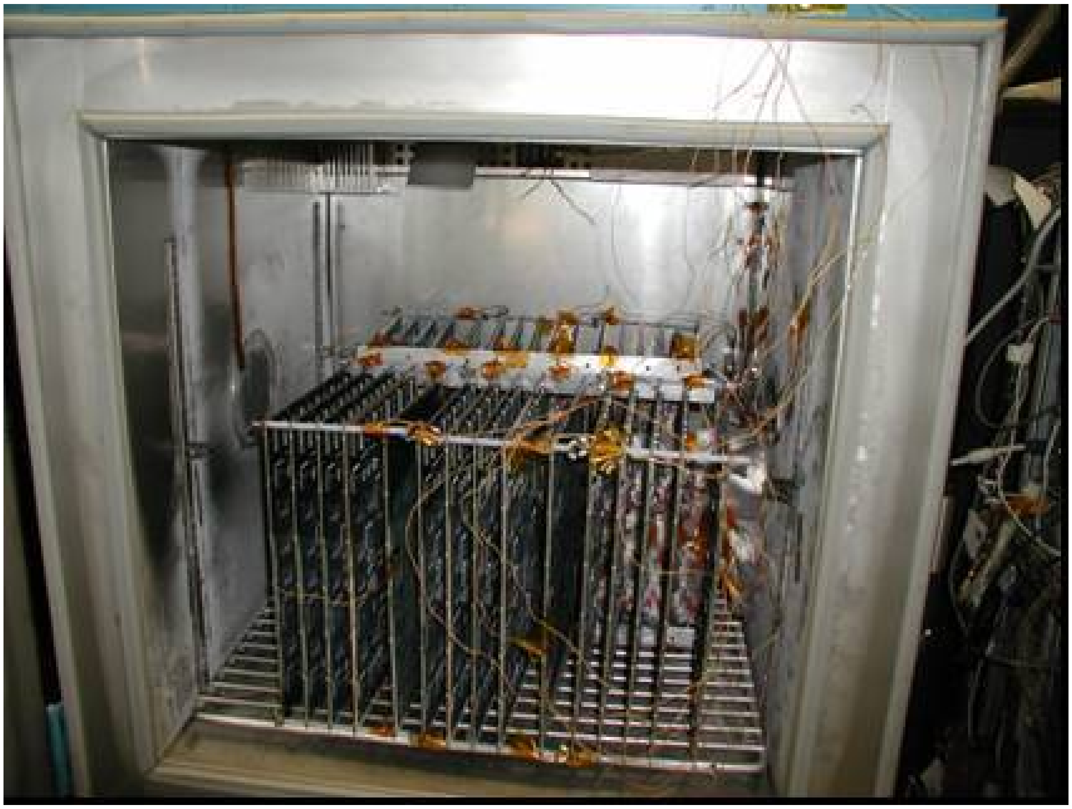


Figure 6 Thermal Cycle Test Chamber

Data Recording and Calculations

- Record data and compare to acceptance criteria as specified in JTP Section 4.1.1.

4.2.4 **Combined Environments Test (CET)**

Description

These tests determine the operational and endurance limits of the PWAs (test vehicles) and solder alloys.

The Combined Environments Test (CET) for the NASA-DoD Lead-Free Electronics Project is based on a modified Highly Accelerated Life Test (HALT), a process in which products are subjected to accelerated environments to find weak links in the design and/or manufacturing process.

The CET process can identify design and process related problems in a much shorter time frame than other development tests. In this project, CET will determine the operation and endurance limits of the solder alloys by subjecting the test vehicles to accelerated environments. The limits identified in CET will be used to compare performance differences in the lead-free test alloys and mixed solder joints vs. the baseline standard SnPb (63/37) alloy. The primary accelerated environments are temperature extremes (both limits and rate of change) and vibration (pseudo-random six degrees of freedom [DOF]) used in combination.

Perform this test in accordance with the following procedure:

- Perform this test utilizing a temperature range of –55 to 125°C with 20°C/minute ramps. The dwell times at each temperature extreme are the times required to stabilize the test sample plus a 15-minute soak. Apply 10 g_{rms} pseudo-random vibration for the duration of the thermal cycle. Continue testing until sufficient data is generated to obtain statistically significant Weibull plots indicating relative solder joint endurance (cycles to failure) rates. If significant failure rates are not evidenced after 50 cycles, increase the vibration levels in increments of 5 g_{rms} and continue cycling for an additional 50 cycles. Repeat this process until all parts have failed or 55 g_{rms} is reached.

Rationale

The project stakeholders felt that Combined Environments Testing would provide a method to identify comparative potential reliability differences in the test alloys vs. the SnPb baseline in a short period of time.

Table 8 Combined Environments Test Methodology

Parameters	- -55°C to +125°C - Number of cycles ≥ 500 - 20°C/minute ramp - 15 minute soak - Vibration for duration of thermal cycle - 10 G_{rms}, initial - Increase 5 Grms after every 50 cycles - 55 G_{rms}, maximum					
Number of Test Vehicles Required						
Manufactured				Rework		
Mfg. SnPb	Mfg. LF	Mfg. LF SN100C	Mfg. LF ENIG	Rwk. SnPb	Rwk. SnPb ENIG	Rwk. LF
5	5	5	1	5	1	5
Trials per Specimens		1				

Major or Unique Equipment
- HALT chamber
- Event detector (Anatech or equivalent)
- Fixture

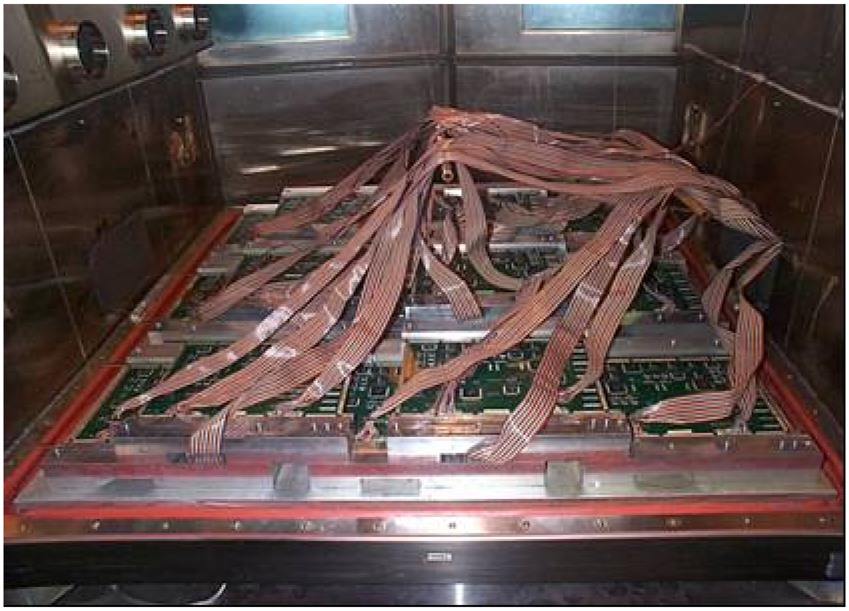


Figure 7 Combined Environments Test Fixture

Data Recording and Calculations
- Record data and compare to acceptance criteria as specified in JTP Section 4.1.1.

4.2.5 Drop Testing

Description

This test determines the resistance of board level interconnects to board strain induced by dynamic bending as a result of drop testing. Boards tested using this method typically fail either as interfacial fractures in the solder joint (most common with ENIG) or as pad cratering in the component substrate and/or board laminate (see Figure 4). These failure modes commonly occur during manufacturing, electrical testing (especially in-circuit test), card handling and field installation. The root cause of these types of failures are typically a combination of excessive applied strain due to process issues and/or or weak interconnects due to process issues and/or the quality of incoming components and/or boards.

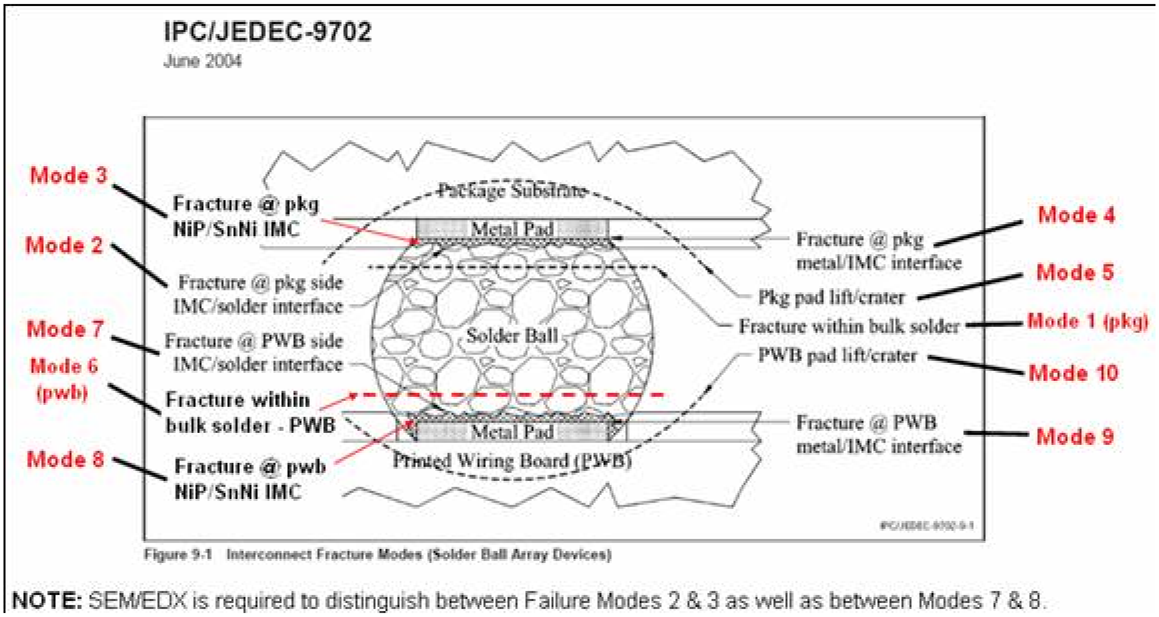

IPC/JEDEC-9702
June 2004
Mode 3
Fracture @ pkg NiP/SnNi IMC
Mode 2
Fracture @ pkg side IMC/solder interface
Mode 7
Fracture @ PWB side IMC/solder interface
Mode 6 (pwb)
Fracture within bulk solder - PWB
Mode 8
Fracture @ pwb NiP/SnNi IMC
Package Substrate
Metal Pad
Solder Ball
Metal Pad
Printed Wiring Board (PWB)
Fracture @ pkg metal/IMC interface
Mode 4
Pkg pad lift/crater
Mode 5
Fracture within bulk solder
Mode 1 (pkg)
PWB pad lift/crater
Mode 10
Fracture @ PWB metal/IMC interface
Mode 9
IPC/JEDEC-9702-9-1

Figure 9-1 Interconnect Fracture Modes (Solder Ball Array Devices)

NOTE: SEM/EDX is required to distinguish between Failure Modes 2 & 3 as well as between Modes 7 & 8.

Figure 4 Interconnect Fracture Modes (Solder Ball Array Device) IPC 9702.

This board-level drop test is based on the JEDEC Standard JESD22-B110A known as Subassembly Mechanical Shock as well as insight gained by Celestica after performing numerous drop tests.

The drop test process can identify design, process, and raw material related problems in a much shorter time frame than other development tests. In this project, the drop test will determine the operation and strain endurance limits of the solder alloys and interconnects by subjecting the test vehicles to accelerated environments. The limits identified in drop testing will be used to compare performance differences in the lead-free test alloys and mixed solder joints vs. the baseline standard SnPb (63/37) alloy. The primary accelerated environments are strain and strain rate.

Rationale

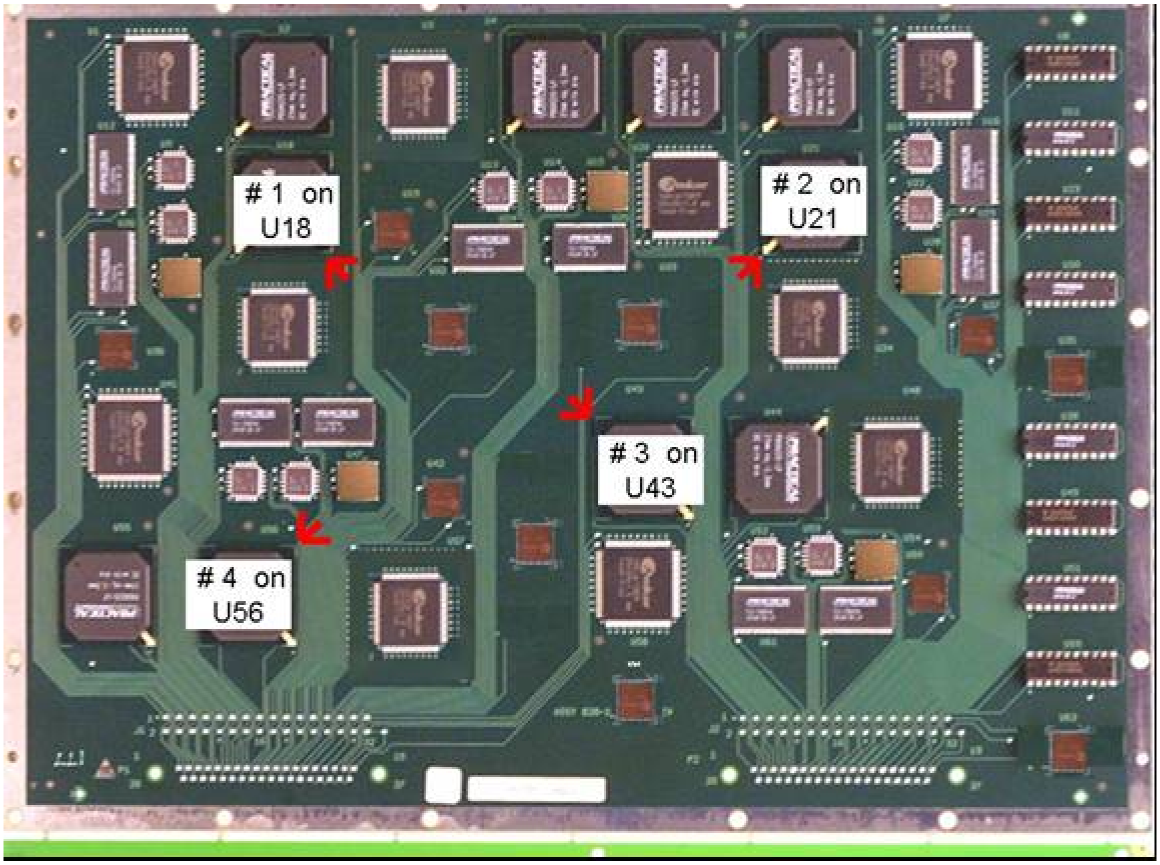
The Drop Testing will provide a method to identify comparative potential quality and reliability differences in the pure and mixed test alloys vs. the SnPb baseline in a short period of time. Unique to this test will be comparing the interconnect robustness of as-assembled to reworked boards. The proposal is to monitor the 3 largest BGAs because previous experience indicates these components fail first.

Resistance monitoring

The high frequency required for monitoring the resistance over the short test period limits the data collection to the 3 nets proposed. (Note: If additional monitoring equipment is available for use by one of the team members, then there can be discussion about potential for additional nets to be monitored. The drop test engineer would need to have some discussion about capabilities of that particular unit and what other resistance nets could/should be monitored)

Strain Gage

- 4 strain gages on one setup card
- 4 strain gages on one card from each of the 5 cells
- The strain data will only be collected and analyzed on the 1st, 5th and 10th drops



Note: strain gages have been placed at the inner most corners of the largest BGAs these area are expected to see the greatest strains. If set-up testing shows something different, the strain gages can be relocated.

Figure 8 Location of the four triaxial strain gages

Table 9 Drop Test Methodology

<table>
<tr><td>Parameters</td><td colspan="4">- Shock testing will be conducted in the -Z direction
- 340Gpk input, 2ms pulse duration
- Test vehicles will be dropped until all monitored components fail or 10 drops have been completed</td></tr>
<tr><td colspan="5">Number of Test Vehicles Required</td></tr>
<tr><td colspan="2">Manufactured</td><td colspan="3">Rework</td></tr>
<tr><td>Mfg. SnPb</td><td>Mfg. LF</td><td>Rwk. SnPb</td><td>Rwk. SnPb ENIG</td><td>Rwk. LF</td></tr>
<tr><td>5</td><td>5</td><td>5</td><td>1</td><td>5</td></tr>
<tr><td>Trials per Specimen</td><td colspan="4">A maximum of 10 drops</td></tr>
</table>

Table 10 Drop Test Results to be Reported

- Input acceleration versus time
- Tabulate results per JEDEC Standard JESD22-B110A
- Output response acceleration with respect to time
- Principal strains (max and min) with respect to time, each rosette
- Individual graphs of strain data for each rosette versus time, with max and min values indicated
- The number of drops until electrical failure (up to 10)

Major or Unique Equipment

- Drop test table
- In-situ electrical resistance monitoring
- Strain gage analysis system
- Fixture
- Depopulated test vehicle assembly and re-sizing

Data Recording and Calculations

- Drop test table – Lansmount Model 65/81 Shock Test System
- Record data and compare to acceptance criteria as specified in JTP Section 4.1.1.
- A daisy-chain resistance increase greater than 10% from the baseline is considered a failure.
- Resistance measurements must be done either in-situ or on the tested assembly while it is under a static load in order to simulate the maximum board flexure observed during the peak acceleration. The actual static load is determined by trial and error based on a sample which failed during in situ resistance monitoring but passes under a non-loading condition, i.e. the crack closes up when the board is not flexed. If electrical testing is performed only after a test, while the board has resumed its neutral bend state, intermittent electrical failures may be overlooked.

4.2.6 **Interconnect Stress Test (IST)**

Description

IST is an industry recognized test method (IPC) that accelerates thermal cycling testing by heating a specifically designed test coupon to 150°C (higher temperatures in specific applications in exactly 3 minutes followed by cooling to ambient in approximately two minutes. IST test coupons have two circuits, a sense circuit and a power circuit, to monitor material delamination and crazing. The power circuit heats the coupon and senses damage accumulation on internal interconnections. The sense circuit is a passive circuit that monitors temperature and measures damage accumulation of the interconnect structure, typically a plated through-hole (PTH). There are usually 400 to 800 structures per circuit to achieve a higher, statistically relevant, sample size. Both the power and sense circuits changes in resistance (milliohms) and temperature (°C) throughout the coupons during the thermal cycle. Thermal cycling continues until end of test or a 10% increase in resistance on either circuit. Each coupon is heated, monitored, and tested individually. This gives a number of advantages that include no hold time at temperature, tight test control in the ability to achieve any test temperature in three minutes +/- 5 seconds, the ability to stop testing within seconds of the circuit achieving a 10% increase in resistance allowing analysis of a developing failure rather than a catastrophic failure. Testing stops immediately when the circuit achieves 10% increase in resistance, allowing a failed circuit to have a low amount of power applied that creates a hot spot at the failure site visible by a thermal imaging camera.

Rationale

The project stakeholders felt that using IST testing provides the advantage of monitoring interconnections (posts) integrity and interconnect structures (PTH) simultaneously, fast and accurate thermal cycling, the ability to stop testing on any failed coupon within seconds, accurate failure location method, failure analysis of a developing failure and latent failure modes, coupons that are intelligently designed to be sensitive to damage accumulation in the structure of interest, evaluation for material degradation, and a statistically acceptable interconnection sample size.

Test Method

1. Coupons are designed to reflect the physical variable of the corresponding circuits' board. The coupons will have one or more power and sense circuits. The coupon will also have a simple registration circuit to qualify misregistration in ranges of 0 to 3, 3 to 5, 5 to7 and 7 to 9 mils. The coupon will have delamination circuits on ground planes allowing the sensing of delamination, crazing, and material decomposition.
2. Coupons are received and subjected to incoming inspection and prescreening. The resistance of each test circuit is measured in milliohms and checked for shorts. The registration circuit is buzzing and the degree of misregistration is determined. Capacitance in picofarads for each ground plane is measured and recorded. The data is subject to standard statistical analysis to include mean, standard deviation (one sigma limit), minimum and maximum, range, and coefficient of variation (mean divided by standard deviation expressed in a percentage). Groups are sorted and selected based on this data. A construction profile is created by plotting the

capacitances of each electrical plane and comparing the results between coupons. Coupons with variation in construction are readily identified and dispositioned. Coupons selected for testing are prepared by soldering four pinheads into the circuits to be tested.

3. Assembly and rework simulation is achieved by subjecting the coupon to heating to 230°C (260°C for lead-free applications) in three minutes followed by cooling to ambient in approximately 2 minutes. Three thermal cycles simulate assembly and six thermal cycles simulate assembly and rework. After preconditioning the coupons are subjected to capacitance measurements and material damage is identified.
4. Testing is performed in the IST tester by heating each coupon individually to 150°C in three minutes +/- five seconds followed by cooling to ambient in approximately two minutes. Testing continues until end of test or a 10% increase in resistance. In DOE type experiments, testing is usually extended until a 50% failure rate is achieved. The IST tester automatically records the testing history for each coupon individually. IST cycles to failure are recorded and subjected to mean, standard deviation, minimum, maximum, range, and coefficient of variation. On occasion Weibull analysis is performed with eta, beta, and MTBF calculated. Weibull plots may be generated to include Weibull Probability and Probability Density Function.
5. The IST data from the testing is used to create a plot of damage accumulation during the life of the test. The resistance measurement at 150°C is plotted for each thermal cycle. The onset, rate of increase and acceleration is easily visualized in “resistance graphs”. Type and severity of failure may be discerned by the damage accumulation in “resistance graphs”.
6. Capacitance measurements in picofarads are measured at the end of test and the percent change from the “as received” condition is calculated. A 4% increase in capacitance is considered significant and subjected to further investigation.
7. Failed coupons (and coupons with suspected delamination) are collected and samples are selected for failure location and microsectioning. Failure location is achieved by subjecting failed circuits (10% increase in resistance) to a small DC current (usually 1-3 amps) while being monitored by a thermal imaging camera. The single most damaged interconnection will appear as the hottest spot in the coupons. The site is identified and subjected to standard cross section preparation. Failure sites are examined and micrographs are generated.
8. Material testing may be indicated when the microsections evaluation find obvious cause for failure. The influence of material IST test results may not be expressed in the microsection and addition material testing may be indicated. Thermal mechanical analysis (TMA) and dynamic mechanical analysis (DMA) may be employed to determine the role of material in failures. TMA data yields the glass transition temperature (Tg), coefficient of thermal expansion (CTE) before and after Tg, and time to delamination. DMA testing yields Young’s Modulus, Tg from the storage, loss moduli, and tan delta.
9. The final step is data analysis and comparison against established databases. Data from control coupons are compared to preconditioned coupons or coupons that have been exposed to other variables. The results are then compared to results from similar testing.

Major or Unique Equipment

- IST tester
- ohmmeter capable of detecting low resistance changes
- Power supply
- Thermal imaging camera
- Dissecting and metallurgical microscopes
- Thermal mechanical analyzer
- Dynamic mechanical analyzer
- Soldering iron, 4 pinheads etc.

Data Recording and Calculations

- The power and sense circuits are monitored for changes in temperature and resistance throughout testing. This is achieved by measuring every circuit every two seconds.
- At incoming inspection coupons are measured for resistance in milliohms on both sense circuits, registration (drill hole to clearance on inner layers), and capacitance in picofarads.
- Copper thickness and hole size is recorded after cross section preparation; micrographs are saved in a .jpg format.
- TMA and DMA data is collected by the respective test equipment.
- Standard and Weibull Statistical analysis is performed with spreadsheet calculations or ReliaSoft Weibull 6++ software.

4.2.7 **Copper Dissolution**

Description

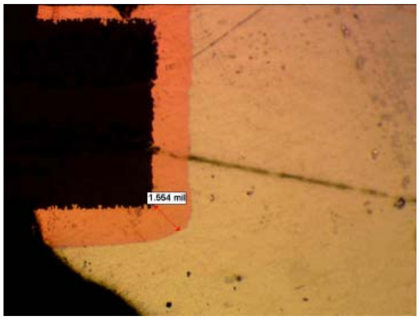
The purpose of the copper dissolution testing is to characterize, document, and compare the impact of soldering process on the copper plated through-hole and surface pad structures for the NASA-DoD test vehicles with the SAC305 and SN100C solder alloy systems. The copper dissolution test results will provide a data set which can be used as a first order approximation of the copper plating thickness loss due to lead-free solder processing. Additionally, the copper dissolution test results can be compared to other published industry results for alternative solder alloy systems and different soldering processes.

Printed Circuit Board (PCB) land and plated through-holes can be eroded or dissolved away in the presence of molten solder rendering the PCB non-functional. Significant dissolution can occur with the use of certain new Sn-rich alloys and is further exacerbated by higher process temperatures. Clearly this phenomenon represents a serious risk to circuit reliability. There is a clear need to determine the dissolution rate of copper pads with lead-free solders under various conditions.

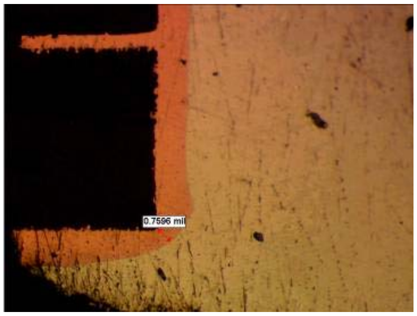
Rationale

The project stakeholders felt that it was important to gain additional data on copper dissolution while developing a testing method that could be used across the industry. The consortium felt that it was important to compare results from SAC solder alloys as well as SN100C since these solder alloys are becoming more common.

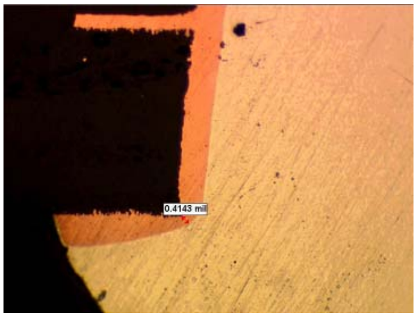
Below are cross sections of plated barrel copper effects at various exposure times to the rework pot using SAC solder.



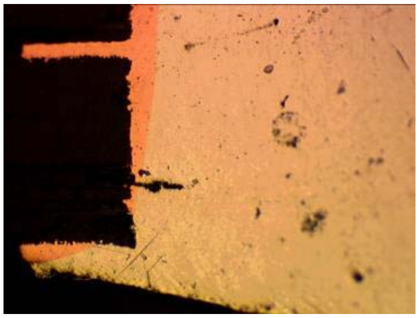
Sample 8: 5 seconds



Sample 13: 13 seconds



Sample 10: 30 seconds



Sample 16: 55 seconds

The coupon features are shown below. The PTH pattern has serial reduction in hole size to simulate the various aspect ratios possible in through-hole soldering and the effects of the barrel (plated copper) when exposed to rework conditions. The surface trace feature (Foil copper) of the coupon has been included to evaluate the effect on surface features exposed to rework.

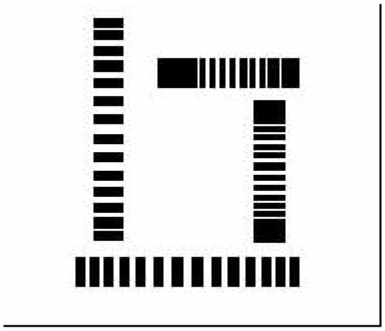


Figure 9 SMT Copper Dissolution Pattern

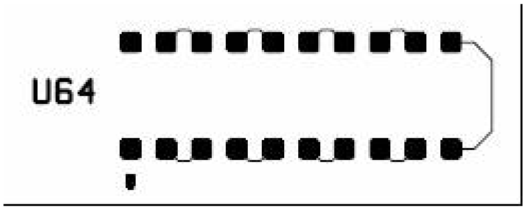


Figure 10 Plated Through-Hole Copper Dissolution Pattern

Table 11 Copper Dissolution Testing

<table>
<tr><td>Parameters</td><td colspan="5">• Mini-wave soldering versus manual soldering
• Number of component removals: 1X versus 3X
• PDIPS on break off coupon and QFP pad pattern
• Metallographic Analysis:
- As fabricated copper thickness
- As assembled copper thickness
- As reworked copper thickness</td></tr>
<tr><td colspan="6">Number of Test Vehicles Break off Coupons Required</td></tr>
<tr><td colspan="3">Manufactured</td><td colspan="3">Rework</td></tr>
<tr><td>Mfg. SnPb</td><td>Mfg. LF</td><td>Mfg. LF SN100C</td><td>Rwk. SnPb</td><td>Rwk. SnPb ENIG</td><td>Rwk. LF</td></tr>
<tr><td>5</td><td>5</td><td>5</td><td>5</td><td>1</td><td>5</td></tr>
</table>

<u>Major or Unique Equipment</u>

- Wave Mini-pot – AirVac or equivalent
- Metcal Solder Iron with 700F tip

Data Recording and Calculations

- Data will be collected via cross sectioning of the sample sites.
- Copper thickness will be reported from SEM measurements.
- Rework alloy exposure time (seconds) will be reported.